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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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7590

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COOK MCFARRON & MANZO LTD
200 WEST ADAMS STREET
SUITE 2850
CHICAGO, IL 60606

EXAMINER

LOKE, STEVEN HO YIN

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 03/15/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/435,154

Applicant(s)

YAMAZAKI ET AL.

Examiner

Steven Loke

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 January 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4, 6-9, 11-17, 19-22 and 24-26 is/are rejected.
- 7) ☒ Claim(s) 5, 10, 18 and 23 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 24.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

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1. Claims 1, 6, 11, 14, 19 and 24 are objected to because of the following informalities:

In claims 1, 6, 14, 19, line 5, "top and side surface" is unclear whether it is being referred to "top and side surfaces".

In claim 6, line 13, it is unclear whether said n-channel TFT does not overlap said first source and drain regions.

In claim 11, lines 12-13, claim 24, lines 10-11, it is unclear whether a second gate electrode formed adjacent to a second semiconductor layer with a second gate insulating film interposed therebetween.

In claim 19, line 13, "said n-channel region" is unclear whether it is being referred to "said n-channel TFT".

Appropriate correction is required.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyasaka et al.

Miyasaka et al. discloses an LDD-type CMOS TFT circuits formed in a LCD device in figs. 26, 49A, 49B. It comprises: an n-channel TFT having LDD regions [9] and source and drain regions [3], a gate electrode [6] partially overlaps the LDD regions [9]; a p-

channel TFT having a third impurity region (source or drain region) [10, 4], a gate electrode [6] partially overlaps the third impurity region [10, 4]; a wiring [8] is connected to the p-type region [10, 4].

It would have been obvious for the LCD device is a ferroelectric LCD device because it is a widely used liquid crystal material.

In regards to claim 12, it would have been obvious to have the claimed materials for the first and second gate electrodes because they are low resistance gate metal materials.

4. Claims 1-4 and 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyasaka et al. in view of Kondo.

Miyasaka et al. differs from the claimed invention by not showing the gate electrode having a first conductive layer and a second conductive layer.

Kondo discloses a gate electrode having a first conductive layer (polysilicon) [4] and a second conductive layer (titanium silicide) [20] being in contact with a gate insulating film [3] and a top surface and side surfaces of the first conductive layer in fig. 1. The second conductive layer [20] partially overlaps the n-type LDD region [6a].

Since both Miyasaka et al. and Kondo teach a gate electrode overlaps the LDD region in a MOSFET, it would have been obvious to have the gate electrode structure of Kondo in each of the TFTs of Miyasaka et al. because it relaxes a concentration of an electric field at the end of the drain.

The p-type regions [10, 4] adjacent to both sides of the gate electrode [6] are considered as the second source and drain regions of claims 1 and 6.

In regards to claims 2, 7, it would have been obvious to have the claimed materials for the first conductive layers of the MOSFETs because they are low resistance gate metal materials.

5. Claims 14-17 and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyasaka et al. in view of Kondo, further in view of Johnson.

Miyasaka et al. and Kondo differ from the claimed invention by not showing the CMOS circuit is used in a goggle type display device.

Johnson shows a goggle type LCD display device having a control circuitry and a display screen [12] in figs. 1 and 2.

Since Miyasaka et al. and Johnson teach a LCD device with control circuitry, it would have been obvious to have the CMOS circuit of Miyasaka et al. in the control circuit of Johnson because it increases the speed of the device.

In regards to claims 15, 20, it would have been obvious to have the claimed materials for the first conductive layers of the MOSFETs because they are low resistance gate metal materials.

6. Claims 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyasaka et al. in view of Johnson.

Miyasaka et al. differs from the claimed invention by not showing the CMOS circuit is used in a goggle type display device.

Johnson shows a goggle type LCD display device having a control circuitry and a display screen [12] in figs. 1 and 2.

Since Miyasaka et al. and Johnson teach a LCD device with control circuitry, it would have been obvious to have the CMOS circuit of Miyasaka et al. in the control circuit of Johnson because it increases the speed of the device.

In regards to claim 25, it would have been obvious to have the claimed materials for the first and second gate electrodes of the MOSFETs because they are low resistance gate metal materials.

7. Applicant's arguments filed 1/9/02 have been fully considered but they are not persuasive.

It is urged, in page 7 of the remarks, that Miyasaka et al. fail to disclose that the second gate electrode in the p-channel TFT partially overlapping the third impurity region that constitutes the source or drain region. However, the region [10, 4] in each of the source and drain areas is considered as a single region. Therefore, the second gate electrode in the p-channel TFT partially overlapping the third impurity region that constitutes the source or drain region.

It is urged, in page 8 of the remarks, that both Miyasaka et al. and Kondo do not expressly teach or suggest the p-channel TFT in which the second conductive layer partially overlaps the source or drain regions. However, the region [10, 4] in each of the source and drain areas of Miyasaka et al. is considered as a single region and the region [(5, 5a), (6, 6a)] in each of the source and drain areas of Kondo is considered as a single region. Therefore, Miyasaka et al. does expressly teach or suggest the p-channel TFT in which the second conductive layer partially overlaps the source or drain regions. In addition, the p-channel complement TFT of Kondo does expressly teach or

suggest the p-channel TFT in which the second conductive layer partially overlaps the source or drain regions.

8. Claims 5, 10, 18 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers

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for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

sl
March 14, 2002

Steven Loke
Primary Examiner

A handwritten signature in cursive script that reads "Steven Loke".